URN etd-0407109-183725-2123
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Statistics This thesis had been viewed 51 times. Download 96 times.
Department
Year 2003
Semester 1
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title An Automatic Layout Generator for I/O Cells
Date of Defense 0000-00-00
Page Count 0

Keyword
Automatic
Cell

Abstract
We present a new design methodology for I/O cell library design automation. It’s different from the conventional cell library compilers or generators, which generate the cells for standard cells or regular structures (e.g., SRAM). The proposed compiler will generate I/O cells based on a set of parameterized unit-cells with the features of scalable geometry dependence. The compilation results of the I/O cells have been proved in a 0.13um LOGIC 1P8M process. Through this compiler, the number of unit-cells needed to be maintained is dramatically reduced, thereby reducing library development costs and time to market.
Advisory Committee Jing-Jou Tang - advisor

Files etd-0407109-183725-2123-001.pdf

indicate access worldwide
Date of Submission 2004-08-06